

TITLE 400G QSFP-DD SR8 Transceiver	DOC No. RFD-20240223010-002	
	REVISION : 01	AUTHORIZED BY : Albert Lin
	DATE : 2025.03.27	CLASSIFICATION : CONFIDENTIAL

1. Description

400G QSFP-DD SR8 is a cost effective module with high performance, which is optimized for Datacenter, supporting data-rate of 8×26.5625 GBd PAM4. Its transmission distance is up to 70m on OM3 MMF. The module mainly consists of two parts: the transmitter part and the receiver part. The transmitter part consists of an 850nm VCSEL array and a driver. The receiver part consists of a trans-impedance amplifier (TIA) and a PIN photodiode array. The high-speed electrical interface is based on low-voltage logic, with nominal 100ohms differential impedance, AC coupled in the module. Users can access a series of registers in transceiver to access monitoring and configuration data through two wire serial interface.

2. Features

- 26.5625 GBd PAM4×8 channel 400G-SR8 Optical interface
- 26.5625 GBd PAM4×8 channel 400G AUI-8C2M Electrical interface
- Up to 70m transmission distance on OM3MMF
- 850nm VCSEL and PIN receiver
- QSFP-DD MSA package with MPO-16-APC
- Very low EMI and excellent ESD protection
- 3.3V power supply
- Power consumption less than 10.5W
- Operating case temperature: 0~70°C
- Fast Tx-Disable & Rx- Los
- IIC rate up to 400KHz

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3. Product Description

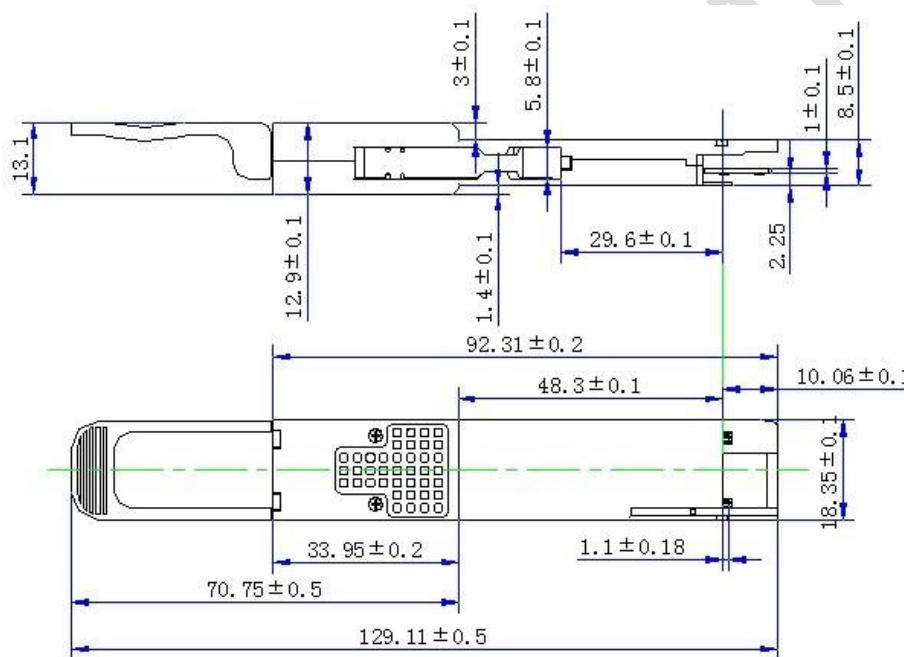
3.1. PRODUCT NAME

400G QSFP-DD SR8 Transceiver

JPC P/N	Wavelength(nm)	Distance	Power(dBm)	Fiber type	Sen.(dBm)	Connector	Temp.
P66**8GRCAS1-1	850	70m (OM3)	-6.5 ~ 4	MMF	-6.5	MPO-12	C

Note-1 : ** Indicates the customer code.

3.2. Dimensions, Materials, Plating and Marking



4. Applications & Compliance

- QSFP-DD MSA
- IEEE 802.3cd
- CMIS Rev4.0
- RoHS compliance

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5. Product Specification

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	TS	-40	85	°C	
Supply Voltage	VCC3	3.1	3.5	V	
Relative Humidity(Non-Condensing)	RH	5	85	%	
Rx Input Power	Pmax		5	dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T _{OPR}	0	-	70	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Current at hot plug	I _{CC_IP}	-	-	3350	mA	
Power Dissipation	PD			10.5	W	
Data Rate per channel (PAM4)			26.5625		GBd	
Signaling Speed Accuracy		-100		100	ppm	
Transmission Distance (OM3)				70	m	
Transmission Distance (OM4)				100	m	

General Optical & Electrical Characteristics (Transmitter)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Center Wavelength	λ _C	840	850	860	nm	-
Spectral Width(RMS)	RMS			0.6	nm	1
Laser Off Power	P _{off}			-30	dBm	-
Average Optical Power	P _{avg}	-6.5		4	dBm	-

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Extinction Ratio	ER	3			dB	-
Transmitter and dispersion eye closure	TDECQ			4.5	dB	-
Outer Optical Modulation Amplitude	OMA _{outer}	-4.5		3		2
RIN _{12OMA}	dB/Hz			-128		-
Encircled flux, each lane	EF	≥ 86% @ 19 μm, ≤ 30% @ 4.5 μm				3
Transition time, each lane (max)				34	ps	-
Optical Return Loss Tolerance				12	dB	-
Operating Data Rate, each lane			26.5625		GBd	-

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Even if the TDECQ<1.4dB, the OMA(min) must exceed this value.
3. If measured into type A1a.2, type A1a.3 or type A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.

Table4-Receiver Operating Characteristic-Optical, Electrical

General Optical & Electrical Characteristics (Receiver)

Parameter	Symbol	Min	Typ.	Max	Units	Notes
Center Wavelength	λ _r	840	850	860	nm	
Damage threshold		5			dBm	
Average receive power		-8.4		4	dBm	Note3
Receiver sensitivity (OMA _{outer})	RS	-	-	-	dBm	Note1、2
Receiver Reflectance				-12	dB	
Differential Data Output Voltage Peak to Peak Swing	V _{opp}			900	mV	
Differential output Impedance	Z _{os}	90	100	110	ohms	
Common Mode Voltage	V _{cm}	-0.35		2.85	V	
Differential output return loss	SDD22	Per OIF CEI-56G-VSR-PAM4 and 400GAUI-8 requirements			dB	
Common Mode to Differential conversion	SDC22,					

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and Differential to Common Mode Conversion	SCD22					
Common Mode Return Loss	SCC22			-2	dB	
Near-end ESMW (Eye symmetry mask Width)	EW6	0.265			UI	
Near-end Eye Height,differentials (Min)	EH6	70			mV	
Far-end ESMW (Eye symmetry mask Width)	EW6	0.2			UI	
Far-end Eye Height,differentials (Min)	EH6	30			mV	

Notes:

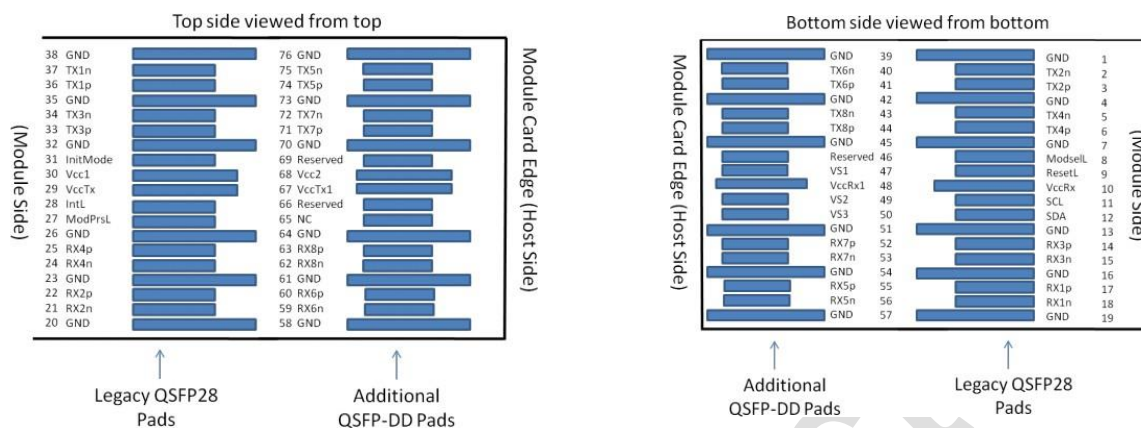
1. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5 dB.
2. $RS = \max(-6.5, SECQ - 7.9)$ (dB)
3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Digital Diagnostic Functions and Control and Status I/O Timing Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	°C	
Tx power monitor absolute error	DMI_TX	-3	3	dB	
Rx power monitor absolute error	DMI_RX	-3	3	dB	
Supply voltage monitor absolute error	DMI_VCC	-3	3	%	
Temperature monitor absolute error	DMI_Temp	-3	3	°C	

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6. Pin Assignments



QSFP-DD Function Definition

Electrical Pin Definition (QSFP-DD)

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	Note1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	Note1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	Note1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	3.3V Power SupplyReceiver	2B	Note2
11	LVCMO S-I/O	SCL	2 wire serial interface clock	3B	
12	LVCMO S-I/O	SDA	2 wire serial interface data	3B	

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13		GND	Ground	1B	Note1
14	CML-O	Rx3n	Transmitter Inverted Data Output	3B	
15	CML-O	Rx3p	Transmitter Non-Inverted Data Output	3B	
16		GND	Ground	1B	Note1
17	CML-O	Rx1n	Transmitter Inverted Data Output	3B	
18	CML-O	Rx1p	Transmitter Non-Inverted Data Output	3B	
19		GND	Ground	1B	Note1
20		GND	Ground	1B	Note1
21	CML-O	Rx2n	Transmitter Inverted Data Output	3B	
22	CML-O	Rx2p	Transmitter Non-Inverted Data Output	3B	
23		GND	Ground	1B	Note1
24	CML-O	Rx4n	Transmitter Inverted Data Output	3B	
25	CML-O	Rx4p	Transmitter Non-Inverted Data Output	3B	
26		GND	Ground	1B	Note1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccRx	3.3V Power Supply Transmitter	2B	Note2
30		VccI	3.3V Power Supply	2B	Note2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	Note1
33	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
34	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
35		GND	Ground	1B	Note1

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36	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
37	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
38		GND	Ground	1B	Note1
39		GND	Ground	1A	Note1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	Note1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	Note1
46		Reserved	NC	3A	Note3
47		VS1	NC	3A	Note3
48		VccRx1	3.3V Power Supply	2A	Note2
49		VS2	NC	3A	Note3
50		VS3	NC	3A	Note3
51		GND	Ground	1A	Note1
52	CML-O	Rx7n	Transmitter Inverted Data Output	3A	
53	CML-O	Rx7p	Transmitter Non-Inverted Data Output	3A	
54		GND	Ground	1A	Note1
55	CML-O	Rx5n	Transmitter Inverted Data Output	3A	
56	CML-O	Rx5p	Transmitter Non-Inverted Data Output	3A	
57		GND	Ground	1A	Note1
58		GND	Ground	1A	Note1
59	CML-O	Rx6n	Transmitter Inverted Data Output	3A	

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60	CML-O	Rx6p	Transmitter Non-Inverted Data Output	3A	
61		GND	Ground	1A	Note1
62	CML-O	Rx8n	Transmitter Inverted Data Output	3A	
63	CML-O	Rx8p	Transmitter Non-Inverted Data Output	3A	
64		GND	Ground	1A	Note1
65		NC	NC	3A	Note3
66		Reserved	NC	3A	Note3
67		VccTx1	3.3V Power Supply	2A	Note2
68		Vcc2	3.3V Power Supply	2A	Note2
69		Reserved	NC	3A	Note3
70		GND	Ground	1A	Note1
71	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
72	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
73		GND	Ground	1A	Note1
74	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
75	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
76		GND	Ground	1A	Note1

Notes:

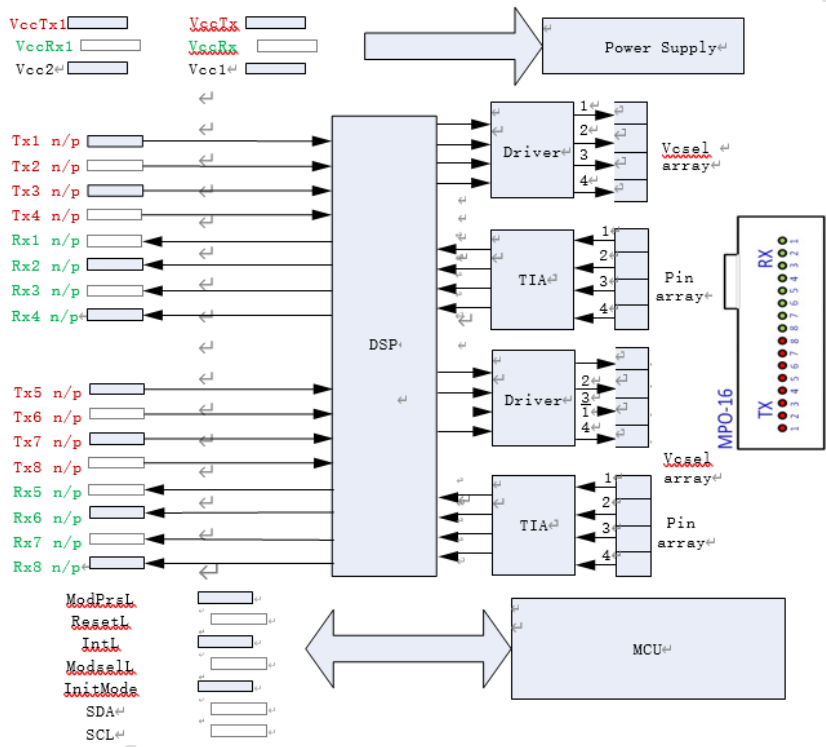
1. QSFP-DD uses common ground (GND) for all signals and supply (power) . All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an

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impedance to GND that is greater than 10kΩ and less than 100pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B,B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

7. Block Diagram of Transceiver



1. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2025/03/27	Albert Lin	Mike Sun